In the Claims:

1. (Cancelled)

2. (Currently Amended) A semiconductor memory device, comprising:

a plurality of unit memory cells, wherein a unit memory cell comprises:

a first planar transistor in a semiconductor substrate;

a vertical transistor disposed on the first planar transistor;

a second planar transistor in the semiconductor substrate, wherein the second planar transistor is electrically connected in series with the first planar transistor;

~~The semiconductor memory device of Claim 1, wherein each unit memory cell further comprises:~~

first and second conductive regions formed in the semiconductor substrate to define a channel region;

a storage node, a multi-junction storage pattern that has first and second sidewalls and a data line, which are sequentially stacked on the semiconductor substrate; and

a word line crossing over the data line and ~~covering~~ on both the first and second sidewalls of the multi-junction storage pattern.

3. (Previously Presented) The semiconductor memory device of Claim 2, wherein the first planar transistor comprises the storage node, the first and second conductive regions and the channel region,

the vertical transistor comprises the word line, the storage node, the data line and the multi-junction storage pattern, and

the second planar transistor comprises the word line, the first and second conductive regions and the channel region.

4. (Previously Presented) The semiconductor memory device of Claim 3, wherein the word line is used as both a gate of the second planar transistor and a gate of the vertical

transistor.

5. (Previously Presented) The semiconductor memory device of Claim 3, wherein the word line is configured to connect the second planar transistors and vertical transistors of the unit memory cells along a direction perpendicular to the data line.

6. (Previously Presented) The semiconductor memory device of Claim 3, wherein the data line is an electrode of the vertical transistor, which is used to supply the storage node with electric charges or to drain electric charge from the storage node.

7. (Previously Presented) The semiconductor memory device of Claim 3, wherein the data line is configured to connect the vertical transistors of the unit memory cells along a direction perpendicular to the word line.

8. (Previously Presented) The semiconductor memory device of Claim 2, a portion of the first conductive region adjacent the channel is lightly doped as compared to a portion of the second conductive region adjacent the channel.

9. (Previously Presented) The semiconductor memory device of Claim 3, wherein the first and second planar transistors are connected in series with the first and second conductive regions.

10. (Previously Presented) The semiconductor memory device of Claim 3, wherein the channel region comprises a first channel region and a second channel region, and wherein the first planar transistor is disposed on the first channel region and the second planar transistor is disposed on the second channel region.

11. (Previously Presented) The semiconductor memory device of Claim 2, further comprising a capping insulation pattern disposed on the data line, the capping insulation pattern separating the data line from the word line.

12. (Currently Amended) The semiconductor memory device of Claim 2[[1]],

wherein the first planar transistor and the second planar transistor have different threshold voltages.

13-37. (Cancelled)

38. (Currently Amended) A semiconductor memory device, comprising:

a source region and a drain region in a semiconductor substrate;

a gate that is laterally offset from at least one of the source region and the drain region and provided on the substrate between the source region and the drain region, wherein the gate comprises the gate of a first planar transistor in the semiconductor substrate;

a vertical transistor on the gate, wherein the vertical transistor comprises the gate which acts as a storage node, a multi-junction storage pattern that has first and second sidewalls, a data line, and a word line which crosses over the data line and which is on both the first and second sidewalls of the multi-junction storage pattern, which are sequentially stacked on the semiconductor substrate; and

a second planar transistor in the semiconductor substrate that is electrically connected in series with the first planar transistor.

39. (Cancelled)

40. (Currently Amended) The semiconductor memory device of Claim 38~~39~~, wherein the storage node comprises a source/drain region of the vertical transistor.

41-44. (Canceled)

45. (Currently Amended) The semiconductor memory device of Claim 2~~1~~, wherein a channel region of the second planar transistor comprises a portion of a channel region of the first planar transistor.

46. (Currently Amended) The semiconductor memory device of Claim 2~~1~~, wherein the first planar transistor and the second planar transistor share a common source/drain

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region.

47-48. (Cancelled)

49. (Currently Amended) The semiconductor memory device of Claim 3848, wherein the word line is used as both a gate of the second planar transistor and a gate of the vertical transistor.

50. (Previously Presented) The semiconductor memory device of Claim 49, wherein the data line is an electrode of the vertical transistor, which is used to supply the storage node with electric charges or to drain electric charge from the storage node.

51. (Previously Presented) The semiconductor memory device of Claim 49, wherein the data line is configured to connect the vertical transistors of the unit memory cells along a direction perpendicular to the word line.

52. (Previously Presented) The semiconductor memory device of Claim 49, wherein the source region and the drain region define a channel region that comprises a first channel region and a second channel region,

wherein the first planar transistor is disposed on the first channel region and the second planar transistor is disposed on the second channel region.

53. (Currently Amended) The semiconductor memory device of Claim 3848, further comprising a capping insulation pattern disposed on the data line, the capping insulation pattern separating the data line from the word line.

54. (Currently Amended) The semiconductor memory device of Claim 3847, wherein the first planar transistor and the second planar transistor have different threshold voltages.